

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): ITO et al.	Atty. Dkt.: 01-543
Serial No.: Unknown	Group Art Unit:
Filed: Concurrently herewith	Examiner:
Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING A SAMPLING SIGNAL GENERATION CIRCUIT	

Commissioner for Patents  
Arlington, VA 22202

Date: January 21, 2004

**INFORMATION DISCLOSURE STATEMENT**

Sir:

Pursuant to 37 C.F.R. §1.56, the reference(s) listed on the attached Form PTO-1449 is/are submitted for consideration by the Examiner without any admission that it/they constitute(s) statutory prior art, or without any admission that it/they contain(s) subject matter that anticipates the invention or renders the invention obvious to a person of ordinary skill in the art.

The Examiner is requested to initial the attached PTO Form-1449 and to return a copy of same to the undersigned attorney as proof that the listed reference(s) has/have been considered and made of record.

Respectfully submitted,



David G. Posz  
Reg. No. 37,701

Posz & Bethards, PLC  
11250 Roger Bacon Drive, Suite 10  
Reston, VA 20190  
(703)707-9110 (phone)  
Customer No. 23400

FORM PTO-1449	ATTY. DKT NO.	01-543	SER. NO.
	APPLICANT	ITO et al.	
	FILING DATE	January 21, 2004	GROUP

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

## FOREIGN PATENT DOCUMENTS

								TRANSLATION	
		DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS	YES	NO
		JP-A-H09-153802* (Discussed in pages 1-2 of the spec.)	06/10/97	JAPAN				X (Abstract)	

\* Full English text is available in machine-translated form in JPO (Japanese Patent Office) English language web site at <http://www1.ipdl.jpo.go.jp/PA1/cgi-bin/PA1INDEX>.

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER		DATE CONSIDERED